a data retrieval channel coupled to receive the transfer extend entries for programming the data transfer.

14. (AMENDED) The data controller of claim 13, wherein the command queueing engine further [includes] comprises a status retrieval channel.

15. (AMENDED) The data controller of claim 14, wherein each of the retrieval channels are coupled to receive transfer extend entries and to provide used read pointers to a first storage device of the peripheral device.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a data controller for use within a peripheral device having a storage medium. The data controller generally comprises a transfer extend generator and at least one retrieval channel. The transfer extend generator may be configured to generate transfer extend entries for a data transfer between the storage medium and a host computer. The at least one retrieval channel may be configured to receive the transfer extend entries for programming the data transfer.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

The Examiner's attention is respectfully directed to the information disclosure statement filed concurrently with this response. The Supplemental IDS includes prior art cited in copending divisional applications, serial numbers 09/223,878 and 09/224,259.

SUPPORT FOR SPECIFICATION AND CLAIM AMENDMENTS

Support for the amendment to the claims may be found, for example, in FIGS. 1-3 as originally filed and, for example, on pages 1-7 and pages 9-11 of the specification, as originally filed. As such, no new matter has been added.

Support for the amendment to the specification may be found in FIG. 4 as originally filed. As such, no new matter has been added.

SPECIFICATION OBJECTION

The specification has been amended as required by the Examiner to correct the reference numbers informalities in: the phrase "DTE read pointer register 440" in page 22, lines 27-28; and the phrase "next free pointer register 440" in page 23, lines 7-8.

The specification has been amended to correct housekeeping which may otherwise be objectionable. As such, no new matter has been added.

CLAIM REJECTION UNDER 35 U.S.C. §112

The rejection to claim 1 under 35 U.S.C. §112, second paragraph has been obviated by appropriate amendment and should be withdrawn. The term "the transfer control entries" has been changed to "the transfer extend entries".

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejections of claims 1 and 5-11, under 35 U.S.C. §102(e) as being anticipated by Garrett et al., U.S. Patent No. 6,049,842, has been obviated by appropriate amendment and should be withdrawn.

Garrett et al. disclose a method for transferring data between non-contiguous buffers in a memory 12 of a host computer and a FIFO 25 of an I/O device 10 via a system bus 14. The method uses a descriptor queue stored in the memory 12. Each descriptor points to a buffer and includes the length of the buffer. When data is to be transferred, a device driver software located in a processor 11 of the host computer sends the number of available descriptors to the I/O device 10. The I/O device 10 then accesses the descriptors individually or in a bust mode to gain access to data within the buffers identified by the descriptors.

In contrast, presently pending claims 1 and 5-11 are directed toward a data controller totally contained within a peripheral device having a storage medium. The data controller

generates transfer extend entries used to program control of data transfers between the storage medium and a host computer. Garrett et al. actually teach away from the present invention by generating the descriptors within the host computer using the device driver software. Garrett et al. are silent as to an apparatus or method for generating the descriptors within the I/O device 10. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

The rejections of claims 2 and 12-13, under 35 U.S.C. §102(b) as being anticipated by Bass et al., U.S. Patent No. 4,262,332, has been obviated by appropriate amendment and should be withdrawn.

Bass et al. disclose a method and mechanism to facilitate a data transfer between a direct access storage device (DASD) 16 and a main memory 12 associated with a central processing unit (CPU) 11 via a channel 13 and a DASD control function device 14. A pair of sequential commands are issued by the CPU 11 to control access to the data in the DASD 16. The first command contains information which defines storage space boundaries of the DASD 16 that the CPU 11 can access. The second command identifies an operation to be carried out within the storage space boundaries defined in the first command and establishes where within the storage space boundary the operation is to take place. The use of

the two commands reduces the amount of involvement by software executed by the CPU 11.

In contrast, presently pending claims 2 and 12-13 are directed toward a data controller within a peripheral device having a processor. The data controller is configured to processes commands from a host computer to minimize interrupts to the processor within the peripheral device. Bass et al. disclose minimizing interrupts between the CPU 11 and devices (i.e., the DASD control function device 14). Bass et al. are silent as to minimizing interrupts to a processor within the DASD control function device 14. Bass et al. minimize the interrupts for a different processor (i.e., CPU 11) than the processor (of the peripheral device) recited in the pending claims. As such the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

The rejections of claims 3 and 16-20, under 35 U.S.C. §102(e) as being anticipated by Born et al., U.S. Patent No. 6,081,849, are respectfully traversed and should be withdrawn.

Born et al. discloses a target device 100 having a controller 101, a CPU 102, a hard disk assembly 110 and a buffer memory 114. The controller 101 can processes multiple commands from a host 140 concurrently. Each command is stored within its own context within the controller 101. When an active command context is prevented from further processing, then an inactive

command context may be swapped with the active command context. Similarly, the active command context may be linked to the inactive command context to automatically swap upon completion of processing to further ease management of multiple contexts. The inactive command context may be read and written by the microprocessor 102 and by swapping with the active command context. The inactive command context may be stored in the controller 101 and/or the buffer memory 114.

In contrast, presently pending claims 3 and 16-20 are directed toward a data controller that is couplable to a host, a storage medium, a microprocessor, a local storage, a buffer memory. The data controller includes a command queuing engine that creates and executes threads of sequential commands while minimizing interrupts associated to the commands. Born et al. disclose creating new command context entries using the CPU 102. Consequently, creation of each new command context requires involvement by the CPU 102. Born et al. actually teach away from creating the command context with the target device controller 101 to minimize the interrupts to the CPU 102. As such the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

The rejection of claim 4, under 35 U.S.C. §102(e) as being anticipated by Krakirian, U.S. Patent No. 5,781,803, has been obviated by appropriate amendment and should be withdrawn.

Krakirian discloses a controller 204 of a SCSI target device 202 comprising a sequencer that causes a SCSI bus to transition from a command bus phase to a data transfer bus phase during execution of an autoread or an autowrite SCSI command without waiting for a communication from a microprocessor 206 of the target device 202. The autoread and the autowrite SCSI commands are carried out by the controller 204 with only two interrupts being generated to the microprocessor 206: one interrupt after receiving the autoread or the autowrite SCSI command from an initiator 201; and one interrupt after a data transfer of the autoread or the autowrite SCSI command is complete.

In contrast, presently pending claim 4 is directed to a peripheral device that includes a data controller, a microprocessor, a buffer memory, a local memory and a storage medium that is couplable to a host. The data controller may create threads of a plurality of commands and generate interrupts at the beginning and end of the plurality of commands relative to a data transfer. Krakirian is silent as to creating threads of sequential commands. Furthermore, Krakirian actually teaches away from interrupting the microprocessor 206 only once at the beginning and once at the end of each thread of multiple commands. As stated in Krakirian column 5, lines 28-33, "an autotransfer (such as an autoread or an autowrite command) is carried out by the disk drive controller integrated circuit with only two interrupts being

generated to the microprocessor: one after receiving the autotransfer command from the initiator; and one after the data transfer of the autotransfer command is complete." Based upon the above reference, a string of N consecutive autotransfer commands from the initiator would result in 2N interrupts to the microprocessor, not just two interrupts. As such the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejections of claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over Bass et al. in view of Garrett et al., has been overcome by appropriate amendment and should be withdrawn.

Presently pending claims 14 and 15 depend from independent claim 2. As argued above, presently pending claim 2 is patentably distinguishable over Bass et al. alone. Assuming, *arguendo*, that combining Bass et al. with Garrett et al. is obvious (for which Applicants' representative does not necessarily agree), then the combination is still silent as to minimizing interrupts to a processor within the DADS control function device 14 (Bass et al.) or the I/O device 10 (Garrett et al.). Since claim 2 is believed to be patentable over the combination of Bass et al. and

Garrett et al. then dependent claims 14 and 15 are also patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 810-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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